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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/909,704
Filing Date: July 20, 2001
Appellant(s): HUFFMAN, WILLIAM A.

Charles S. Fish (Reg. No. 35,870)
For Appellant

EXAMINER'S ANSWER

This is in response to the substitute Appeal Brief filed on 19th of July 2006 appealing from the Office action mailed on 24th of June 2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

US 6,160,812 A	Bauman et al.	12-2000
US 6,185,672 B1	Trull	2-2001
US 6,145,061 A	Garcia et al.	11-2000
US 5,375,223 A	Meyers et al.	12-1994

In re Yount, 36 C.C.P.A. (Patents) 775, 171 F2.2d 317, 80 USPQ 141

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-3 and 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bauman et al. [US 6,160,812 A; hereinafter Bauman] in view of Trull [US 6,185,672 B1]

Referring to claim 1, Bauman discloses a method of managing an arbitration queue (i.e., requests queues 252, 254, 256, 258, and primary arbitration queues 282, 284, 286, 288 in Fig. 17; See col. 3, lines 30-35) having a plurality of queue entries (i.e., requests; See col. 16, lines 37-44) comprising:

- introducing entries (i.e., requests) into said queue at a time-ordered queue location (See col. 16, lines 44-52);
- associating each entry after placement in said queue (i.e., said requests are placed (viz., enqueued) into said queue before being grouped into channel module's request buffer) to one of a plurality of groups (i.e., each entry being associated with one of channel modules, which has a group of requests for primary arbitration; See col. 8, lines 15-32),
    - each of said plurality of groups (i.e., requests group per said channel module) having a different transaction parameter criteria (i.e., different packet priority schemes, e.g., based on the time, or a factor other than time; See col. 8, lines 15-44);
- determining which particular one of said plurality of groups to service (i.e., determining which channel module to be granted by IGRANT_CHN in Fig. 7) based on said transaction parameter criteria (See col. 8, line 60 through col. 9, line 3); and
- servicing a particular entry in said particular one of said plurality of groups based on servicing criteria (i.e., one of requests being granted by IGRANT_CHN is operating

based on said packet priority being set by LEVEL_SEL in Fig. 7; See col. 10, lines 26-37).

Bauman does not expressly teach introducing said entries into said queue at a first, highest order queue location; determining if lower order queue locations are available; moving all higher order queue location contents to an adjacent lower order queue location per cycle until all lower order locations are filled if lower order instruction queue if queue locations are available; and moving all higher order queue entries, with respect to said particular entry being serviced, to an adjacent lower order location in said queue.

Trull discloses a method and apparatus for out-of-order instruction dispatch and queue compaction (See Abstract), wherein

- introducing entries (i.e., new instructions) into queue (i.e., instruction queue 314 in Figs. 8B-C) at a first, highest order queue location (i.e., "top" or start of the queue; See col. 4, lines 31-32);
- determining if lower order queue locations are available (See col. 26, lines 24-27);
    - if lower order queue locations (i.e., lower order lines, where the three instructions are allocated a "line" of instruction storage locations, e.g., storage locations 200, 202, 204, 206, 208, 210 in Fig. 8A; See col. 14, lines 22-24) are available, moving all higher order queue location (i.e., all higher order lines in Figs. 8A-C) contents to an adjacent lower order queue location (i.e., adjacent lower order line of instruction storage locations 200, 202 and 204 in Figs. 8A-C) per cycle (i.e., per compression cycle; See col. 20, lines 19-38) until all lower order locations are filled (See col. 4, lines 33-42);
- servicing a particular entry (i.e., an instruction to be dispatched to processor pipe) in said queue based on servicing criteria (See col. 14, lines 36-51); and

- moving all higher order queue entries, with respect to said particular entry being serviced, to an adjacent lower order location (i.e., lower order line) in said queue (See col. 18, line 61 through col. 19, line 24).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said method of queuing operation with said queue compaction, as disclosed by Trull, in said method of managing said arbitration queue, as disclosed by Bauman, for the advantage of providing said arbitration queue configured to service transactions (i.e., dispatch instructions) in an out-of-order fashion (i.e., an entry can be removed from any location in the queue) and perform collapse of queue entries (i.e., compaction of strings) of empty storage locations (See Trull, col. 3, lines 48-62 and col. 4, lines 20-23).

Referring to claim 2, Trull teaches

- the step of marking a location of a serviced entry (i.e., marking 'clear bit' as setting empty bit; See col. 18, lines 10-13) as idle (i.e., empty; See block 262A of Fig. 11B and col. 21, lines 63-67).

Referring to claim 3, Trull teaches said moving step further comprising

- for higher order locations with respect to said idle location (i.e., empty storage location), writing the contents of higher order queue locations into adjacent lower order queue locations (i.e., shift one row down; See Block 262D of Fig. 11B and col. 22, lines 19-26); and
- for lower order locations with respect to said idle location, rewriting the current entry into said location (i.e., no shift operation; See Block 262C of Fig. 11B and col. 22, lines 26-30; Note - the embodiment of Fig. 8A has a null logic as the new value logic in Fig. 9D).

Referring to claim 5, Trull teaches

- providing a plurality of registers (i.e., instruction storage locations 200, 206, 212, 218, 224, 230 and 236 in Fig. 8B-C) corresponding to a number of entries in said queue (i.e., a number of instructions in said instruction queue 314 in Figs. 8B-C; See col. 5, lines 7-10), said plurality of registers being arranged in a linear array (i.e., instruction storage locations of each column being arranged in a linear array in Figs. 8B-C) from a highest order register (i.e., a highest order storage location, e.g., storage location 236 in Figs. 8B-C) to a lower order register (i.e., a lower order storage location, e.g., storage location 200 in Figs. 8B-C);
- for each register (i.e., for each instruction storage location), selectively providing to each register an entry from that register or an entry from a higher order register (See Fig. 8A and col. 18, line 63 through col. 19, line 2).

Referring to claim 6, Trull teaches said plurality of registers (i.e., instruction storage locations 200, 206, 212, 218, 224, 230 and 236 in Fig. 8B-C) includes

- entries (i.e., new instructions) are added to said queue via said highest order register (See Figs. 3A, 3B, 11A and col. 21, lines 54-61).

Referring to claim 7, Trull teaches said plurality of registers (i.e., instruction storage locations 200, 206, 212, 218, 224, 230 and 236 in Fig. 8B-C)

- each have an entry output such that an entry can be removed from any location in said queue (See col. 21, lines 37-41).

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bauman [US 6,160,812 A] in view of Trull [US 6,185,672 B1] as applied to claims 1-3 and 5-7 above, and further in view of what was well known in the art, as exemplified by Garcia et al. [US 6,145,061 A; hereinafter Garcia]

Referring to claim 4, Bauman, as modified by Trull, discloses all the limitations of the claim 4, except that does not teach the step of initializing all queue locations to an idle state prior to the step of introducing entries into said queue.

The Examiner takes Official Notice that initializing all queue locations to an idle state prior to introducing entries into said queue, is well known to one of ordinary skill in the art, as evidenced by Garcia (i.e., initializing by zeroing all the entries prior to moving data from the old queue into a new queue; See Garcia, col. 2, line 54 through col. 3, line 13).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have been initializing all queue locations (i.e., instruction storage locations) to an idle state (i.e., empty) prior to introducing entries into said queue (i.e., inputting instructions into instruction queue) since it would have obviate any potential malfunction by garbage data (i.e., floating data in the queue after the queue creation and/or power-on operation) in the queue.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bauman [US 6,160,812 A] in view of Trull [US 6,185,672 B1] as applied to claims 1-3 and 5-7 above, and further in view of Case Law, In re Yount, 36 C.C.P.A. (Patents) 775, 171 F2.2d 317, 80 USPQ 141

Referring to claim 8, Bauman, as modified by Trull, discloses all the limitations of the claim 8, including said plurality of registers (i.e., instruction storage locations 200, 206, 212, 218,

224, 230 and 236 in Fig. 8B-C; Trull) having 21 registers (i.e., 7 instruction storage locations; Trull), except that does not expressly teach said plurality of registers having 64 registers.

However, the claim recites said 64 registers without any patentable advantage in the specification (See claim 8 and Application page 12, lines 1-4), such as the reason of "said plurality of registers including 64 registers instead of 7 registers, 21 registers, 32 registers or 128 registers" with any patentable advantage.

Therefore, the limitation of "said plurality of registers including 64 registers" in the claim is not patentably significant since it at most relates to the flexible number of registers under consideration which is not ordinarily a matter of invention. *In re Yount, 36 C.C.P.A. (Patents) 775, 171 F2.2d 317, 80 USPQ 141.*

Claims 9-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Meyers et al. [US 5,375,223 A; cited by the Appellant; hereinafter Meyers] in view of Bauman [US 6,160,812 A] and Trull [US 6,185,672 B1]

Referring to claim 9, Meyers discloses a computer system (i.e., multiprocessor data processing system in Fig. 1) comprising:

- a distributed shared memory system (i.e., main memory 300 of Fig. 1);
- a plurality of processors (i.e., Processors 100 in Fig. 1) generating transactions to said distributed shared memory system (See col. 3, lines 41-48); and
- a memory interface (i.e., memory access circuit 200 of Fig. 1) interposed between said distributed shared memory system and said plurality of processors (See Fig. 1; i.e., Memory Access circuit 200 interposed between Processors 100 and Main Memory 300 in Fig. 1), said memory interface having
    - cache memory (i.e., Cache (L2) 220 of Fig. 1);

- an arbitration queue (i.e., Q 215 of Fig. 1) having a plurality of entry locations (i.e., n multi-bits positions in register 250 in Fig. 8), and
- a memory arbitration processor (i.e., control logic 212 of Fig. 1) for servicing transactions from said plurality of processors (See col. 4, line 61 through col. 5, line 38),
    - said memory arbitration processor performing a memory arbitration scheme (See Fig. 2, col. 4, lines 55-60 and col. 7, line 29 through col. 8, line 32).

Meyer does not teach placing transactions as entries in said arbitration queue; associating entries after placement in said arbitration queue to one of a plurality of groups, each of said plurality of groups having a different transaction parameter criteria; determining which particular one of said plurality of groups to service based on said transaction parameter criteria; and servicing a particular entry in said particular one of said plurality of groups.

Bauman discloses an apparatus for supplying requests to a scheduler (See Abstract and Fig. 17), wherein means for managing an arbitration queue (i.e., requests queues 252, 254, 256, 258, and primary arbitration queues 282, 284, 286, 288 in Fig. 17) comprising

- placing transactions as entries (i.e., requests) in said arbitration queue (See col. 16, lines 44-52);
- associating entries after placement in said arbitration queue (i.e., said requests are placed (viz., enqueued) into said arbitration queue before being grouped into channel module's request buffer) to one of a plurality of groups (i.e., each entry being associated with one of channel modules, which has a group of requests for primary arbitration; See col. 8, lines 15-32),

- each of said plurality of groups (i.e., requests group per said channel module) having a different transaction parameter criteria (i.e., different packet priority schemes, e.g., based on the time, or a factor other than time; See col. 8, lines 15-44);

- determining which particular one of said plurality of groups to service (i.e., determining which channel module to be granted by IGRANT_CHN in Fig. 7) based on said transaction parameter criteria (See col. 8, line 60 through col. 9, line 3); and
- servicing a particular entry in said particular one of said plurality of groups (i.e., one of requests being granted by IGRANT_CHN is operating based on said packet priority being set by LEVEL_SEL in Fig. 7; See col. 10, lines 26-37).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said means for managing said arbitration queue, as disclosed by Bauman, in said memory arbitration scheme, as disclosed by Meyer, for the advantage of said memory arbitration scheme (i.e., arbitration method) being that said memory arbitration processor (i.e., primary scheduler) is presented with a more diverse said arbitration queue (i.e., primary arbitration queue) from which to select transactions (i.e., packets) for transfer through said memory interface (i.e., switch; See Bauman, col. lines 5-8).

Meyer, as modified by Bauman, does not teach said arbitration queue is collapsible and said memory arbitration scheme further comprising: marking a location of said particular entry in said arbitration queue as idle; and collapsing said arbitration queue by bringing all higher order entries into adjacent lower order locations in said queue to fill said idle location.

Trull discloses an apparatus for instruction queue compression (See Abstract and col. 1, lines 6-8), wherein

- an arbitration queue (i.e., instruction queue 160 of Fig. 3A) is collapsible (i.e., compaction process; See col. 4, lines 39-42) and
- a memory arbitration scheme (i.e., managing an instruction queue; See col. 5, lines 4-21) comprising:
    - servicing at least one entry in said arbitration queue (i.e., an instruction to be dispatched to processor pipe; See col. 14, lines 36-51);
    - marking a location of said particular entry in said arbitration queue (i.e., marking 'clear bit' as setting empty bit; See col. 18, lines 10-13) as idle (i.e., empty; See block 262A of Fig. 11B and col. 21, lines 63-67); and
    - collapsing said arbitration queue (i.e., compaction process) by bringing all higher order entries (i.e., all higher order instructions in Figs. 8A-C) into adjacent lower order locations (i.e., adjacent lower order lines of instruction storage locations composed of 3 columns in Figs. 8A-C) in said queue to fill an idle location (i.e., shifting down to adjacent lower order line and filling empty location; See col. 18, line 61 through col. 19, line 24).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted said collapsible arbitration queue and said memory arbitration scheme, as disclosed by Trull, for said arbitration queue and memory arbitration scheme, as disclosed by Meyer, as modified by Bauman, for the advantage of providing said arbitration queue configured to service transactions (i.e., dispatch instructions) in an out-of-order fashion (i.e., an entry can be removed from any location in the queue) and perform collapse of queue entries (i.e., compaction of strings) of said idle locations (i.e., empty storage locations; See Trull, col. 3, lines 48-62 and col. 4, lines 20-23).

Referring to claim 10, Trull teaches said collapsing operation comprises:

- for higher order queue locations with respect to said idle location (i.e., empty storage location), writing the contents of higher order queue locations into adjacent lower order queue locations (i.e., shift one row down; See Block 262D of Fig. 11B and col. 22, lines 19-26); and
- for lower order queue locations with respect to said idle location, rewriting the current entry into said location (i.e., no shift operation; See Block 262C of Fig. 11B and col. 22, lines 26-30; Note - the embodiment of Fig. 8A has a null logic as the new value logic in Fig. 9D).

Referring to claim 11, Trull teaches said plurality of entry locations (i.e., instruction storage locations 200, 202, 204, ... 236, 238, 240 in Fig. 8B) includes

- a highest order location (i.e., instruction storage locations 236, 238, 240 in Fig. 8B) and a lowest order location (i.e., instruction storage locations 200, 202, 204 in Fig. 8B), and wherein
    - entries (i.e., new instructions) are added to said queue via said highest order location (See Figs. 3A, 3B, 11A and col. 21, lines 54-61).

Referring to claim 12, Trull teaches said arbitration queue (i.e., instruction queue 160 of Fig. 3A) comprising

- a plurality of registers (i.e., instruction storage locations 200, 202, 204, 206, 208, 210 in Fig. 8A) corresponding to the number of entries in said queue (See col. 5, lines 7-10);
- a plurality of 2:1 multiplexers (i.e., multiplexers 250, 252, 254, 256, 258, 260 in Fig. 8A) interposed between said registers (See Fig. 8A) such that

- one multiplexer is interposed between a higher order register and a subsequent register (e.g., a multiplexer 250 is interposed between a higher instruction storage location 206 and a subsequent instruction storage location 200 in Fig. 8A),
- the output of said higher order register (e.g., output from instruction storage location 206 in Fig. 8A) being coupled to a first input of said one multiplexer (i.e., an input of multiplexer 250 in Fig. 8A),
- the output of said subsequent register (i.e., output from instruction storage location 200 in Fig. 8A) being coupled to a second input of said one multiplexer (i.e., another input of multiplexer 250 in Fig. 8A),
- an output of said one multiplexer being coupled to said subsequent register (i.e., an output of multiplexer 250 is coupled to instruction storage location 200 in Fig. 8A), and
- a mux control line (i.e., SHIFT_ROW_1 in Fig. 8A) being coupled to said one multiplexer to direct the contents of one of said first and second multiplexer inputs to said multiplexer output (See col. 18, line 63 through col. 19, line 2).

However, the recitation in the claim "whereby the mux control line associated with the higher order register and subsequent register determines whether the subsequent register is refreshed with its current contents or receives the contents of the higher order register" has not been given patentable weight because it has been held that the functional "whereby" statement does not define any structure and accordingly cannot serve to distinguish. *In re Mason, 114 USPQ 127, 44 CCPA 937 (1957).*

Referring to claim 13, Trull teaches said plurality of registers (i.e., instruction storage locations 200, 202, 204, ... 236, 238, 240 in Fig. 8B) includes

- a highest order register (i.e., instruction storage locations 236, 238, 240 in Fig. 8B) and a lowest order register (i.e., instruction storage locations 200, 202, 204 in Fig. 8B), and wherein
    - o entries (i.e., new instructions) are added to said queue via said highest order register (See Figs. 3A, 3B, 11A and col. 21, lines 54-61).

Referring to claim 14, Trull teaches said plurality of registers (i.e., instruction storage locations 200, 202, 204, ... 236, 238, 240 in Fig. 8B)

- each have an entry output such that an entry can be removed from any location in said queue (See col. 21, lines 37-41).

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Meyers [US 5,375,223 A] in view of Bauman [US 6,160,812 A] and Trull [US 6,185,672 B1] as applied to claims 9-14 above, and further in view of Case Law, In re Yount, 36 C.C.P.A. (Patents) 775, 171 F2.2d 317, 80 USPQ 141

Referring to claim 15, Meyers, as modified by Bauman and Trull, discloses all the limitations of the claim 15, including said plurality of registers (i.e., instruction storage locations 200, 202, 204, ... 236, 238, 240 in Fig. 8B; Trull) having 21 registers (i.e., 21 instruction storage locations; Trull), except that does not expressly teach said plurality of registers having 64 registers.

However, the claim recites said 64 registers without any patentable advantage in the specification (See claim 15 and Application page 12, lines 1-4), such as the reason of "said

plurality of registers including 64 registers instead of 21 registers, 32 registers or 128 registers" with any patentable advantage. Therefore, the limitation of "said plurality of registers including 64 registers" in the claim is not patentably significant since it at most relates to the flexible number of registers under consideration which is not ordinarily a matter of invention. *In re Yount, 36 C.C.P.A. (Patents) 775, 171 F2.2d 317, 80 USPQ 141.*

(10) Response to Argument

In response to the Appellant's arguments with respect to "Claims 1-3 and 5-7 stand rejected under 35 U.S.C. §103(a) as being obvious over Bauman, et al. in view of Trull. ..." in the substitute Appeal Brief, pages 7-11, the Examiner respectfully disagrees.

At first, the Appellant states as if Trull discloses an instruction queue that remotely operates, on page 7, lines 18-20. However, Trull never discloses said instruction queue that remotely operates, and further, the Appellant fails to explicitly point out the portion of disclosure in Trull, which can support the Appellant's assertion.

In addition, the Appellant states as if Bauman discloses four registers may operate separately as priority registers where the highest priority register will output its contents in a FIFO manner before contents from a lower priority buffer, on page 7, lines 22-27. However, Bauman never discloses the highest priority register in said four registers, where operate separately as priority registers, will output its contents in a FIFO manner before contents from a lower priority buffer, and further, the Appellant fails to explicitly point out the portion of disclosure in Bauman, which can support the Appellant's assertion.

At second, the Appellant asserts that there is no suggestion or motivation in Bauman or Trull to combine them as proposed by the Examiner, on page 7, line 7 through page 8, line 4.

In particular, the Appellant argues that the Examiner has not cited any language within Bauman or Trull that would suggest any capability for them to be combined, on page 7, line 27 through page 8, line 4.

In contrary to the Appellant's arguments as is stated above, all the rejections under 35 USC §103(a) in the prior Office Actions established a *prima facie* case of obviousness meeting the three basic criteria of the MPEP 2143.03 (8th ed. 2001). Furthermore, the Examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

In this case, the Examiner has clearly pointed out rationale for appropriate combination of Bauman and Trull, such that the combination of Bauman and Trull is for the advantage of providing arbitration queue configured to service transactions (i.e., dispatch instructions) in an out-of-order fashion (i.e., an entry can be removed from any location in the queue) and perform collapse of queue entries (i.e., compaction of strings) of empty storage locations (See Trull, col. 3, lines 48-62 and col. 4, lines 20-23). Therefore, it is clear that the Examiner has cited language of Trull that would properly provide the motivation for the combination.

Even though the Appellant asserts that the Examiner does not suggest any capability for them to be combined, the Examiner notices that the test for obviousness is not whether the features of a secondary reference Trull may be bodily incorporated into the structure of the primary reference Bauman; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references

Bauman and Trull would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

Moreover, the Appellant merely argues that the Examiner's citation from Trull has no commonality with the operation provided in Bauman, and the rationale provided by the Examiner for the combination of Bauman and Trull is purely subjective and speculation with no objective reasoning being provided to support combining the references as has been proposed. However, the Appellant fails to provide any objective reasoning to support the Appellant's argument, as is described above.

In contrary to the above Appellant's mere argument, the Examiner cited Trull for properly supporting the motivation for the combination of Bauman and Trull with commonality, such that it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included a method of queuing operation with queue compaction, as disclosed by Trull, in a method of managing arbitration queue, as disclosed by Bauman, for the advantage of providing said arbitration queue configured to service transactions (i.e., dispatch instructions) in an out-of-order fashion (i.e., an entry can be removed from any location in the queue) and perform collapse of queue entries (i.e., compaction of strings) of empty storage locations (See Trull, col. 3, lines 48-62 and col. 4, lines 20-23).

Thus, Appellant's argument for this point cannot be seen as persuasive.

At third, the Appellant argues that the Examiner's conclusion of obviousness is based upon improper hindsight reconstruction without any support for such conclusively statements from any of the cited references, viz., improper hindsight reasoning, on page 8, lines 4-13. However, the Examiner notices that it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed

invention was made, and does not include knowledge gleaned only from the Appellant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

In this case, the Examiner clearly shows that the combination of Bauman and Trull suggests all the claimed limitations, i.e., the obviousness of the claimed invention, using the claiming language and the references' own language, and further properly provides the motivation for the combination of Bauman and Trull, as is mentioned above.

Therefore, the Examiner believes that a proper reasoning for the combination has been provided in the prior Office Actions, and the burden to establish the first criteria of the *prima facie* case of obviousness has been met.

Furthermore, the Examiner believes that the Appellant misunderstands the paragraph on page 15, lines 21-24 in the Examiner's Answer mailed on 17th of January 2006, i.e., the Appellant asserts that the Examiner readily admits that the claim language was used in supporting the combination of the Bauman and Trull.

In fact, the Examiner states in said Examiner's Answer that the obviousness of the claimed invention was suggested by the combination of Bauman and Trull, and it was evidently shown by way of the mapping between the claiming language and the references' own language. In contrary to the Appellant's assertion, the Examiner has never admitted that the claim language was used in supporting the combination of the Bauman and Trull.

Thus, Appellant's argument for this point cannot be seen as persuasive.

At fourth, the Appellant asserts that the proposed modification changes the principle of operation of the prior art being modified, on page 8, lines 14-30.

In fact, Bauman discloses a method of managing an arbitration queue (i.e., requests queues 252, 254, 256, 258, and primary arbitration queues 282, 284, 286, 288 in Fig. 17; See col. 3,

lines 30-35) having a plurality of queue entries (i.e., requests; See col. 16, lines 37-44), and Trull discloses a method for out-of-order instruction dispatch and queue compaction (See Abstract).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said method of queuing operation with said queue compaction, as disclosed by Trull, in said method of managing said arbitration queue, as disclosed by Bauman, for the advantage of providing said arbitration queue configured to service transactions (i.e., dispatch instructions) in an out-of-order fashion (i.e., an entry can be removed from any location in the queue) and perform collapse of queue entries (i.e., compaction of strings) of empty storage locations (See Trull, col. 3, lines 48-62 and col. 4, lines 20-23).

Actually, the Appellant argues that the Examiner has yet to explain how Bauman and Trull can be combined in view of their different functionalities, viz., their own functionalities, however, the test for obviousness is not whether the features of a secondary reference Trull may be bodily incorporated into the structure of the primary reference Bauman; nor is it that the claimed invention must be expressly suggested in any one or all of the references Bauman and Trull. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). In this case, the Examiner believes that it is obvious to one of the ordinary skill in the art that Bauman's method of managing arbitration queue could include Trull's method of queuing operation with queue compaction in order to provide said arbitration queue configured to service transactions in an out-of-order fashion and perform collapse of queue entries of empty storage locations. Furthermore, it is clear to one of the ordinary skill in the art that the proposed modification doesn't change the principle of operation of Bauman's method of managing arbitration queue being modified by Trull's method of queuing operation with queue compaction

since the principle of operation of Bauman's method could be still performing its own objective of Bauman's invention after the proposed modification.

In addition, the Appellant argues that the Examiner provides a subjective opinion for showing the obviousness of the claimed invention without being supported by any objective evidence. However, in contrary to the Appellant's allegation, the Examiner provides an objective evidence, i.e., Bauman and Trull's disclosure, in order to show the obviousness of the claimed invention (See the item (9) Grounds of Rejection).

Thus, Appellant's argument for this point cannot be seen as persuasive.

At fifth, the Appellant asserts that a reasonable expectation of success has not been shown by the Examiner, on page 8, line 31 through page 9, line 10.

Actually, the Appellant asserts that the Examiner has not addressed how the proposed combination of Bauman and Trull would have any success whatsoever let alone a reasonable expectation of success without the improper hindsight look through the claimed invention. However, in contrary to the Appellant's assertion, the Examiner's conclusion of obviousness is not based upon improper hindsight reasoning, as is explained above.

Furthermore, with regard to the Appellant's argument, i.e., the Bauman would not be able to have the option of either a request buffer with registers combined into a single FIFO unit or separate FIFO priority registers through incorporation of the instruction queue of the Trull, the Examiner believes that the Appellant misinterprets the claim rejection under 35 U.S.C. 103(a) as being unpatentable over Bauman in view of Trull. In fact, the Examiner clearly states that it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included a method of queuing operation with queue compaction, as disclosed by Trull, in a method of managing arbitration queue, as disclosed by Bauman, for the advantage of providing said arbitration queue configured to service transactions (i.e., dispatch instructions) in an out-of-

order fashion (i.e., an entry can be removed from any location in the queue) and perform collapse of queue entries (i.e., compaction of strings) of empty storage locations (See Trull, col. 3, lines 48-62 and col. 4, lines 20-23). In other words, Trull's method of queuing operation with queue compaction is included in Bauman's method of managing arbitration queue for the advantage of performing collapse of queue entries of empty storage locations (i.e., queue compaction), which is in contrary to the Appellant's misinterpretation of the claim rejection such as "Bauman is combined with Trull through incorporation of the instruction queue of Trull with single FIFO unit or separate FIFO priority registers of Bauman."

Finally, the Examiner finds that there would have been a reasonable expectation of success because the prior art Trull teaches that the Appellant's preferred collapsible arbitration queue is efficient to reduce or eliminate the bubbles of empty storage locations form in the queue at col. 4, lines 34-38, and provides better results compared with other prior art's queue compaction, e.g., full compaction (See Trull, col. 18, lines 20-36). In addition, the Appellant fails to present any evidence showing there was no reasonable expectation of success. See MPEP 2143.02. Thus, Appellant's argument for this point cannot be seen as persuasive.

At sixth, the Appellant argues that the Examiner has not shown that the proposed Bauman and Trull combination teaches or suggests all of the claimed limitations, on page 9, line 22 through page 10, line 12.

The Examiner notices that the Appellant brings a new language "FIFO register priority scheme," which was not stated in the prior Appeal Brief filed on 28th of November 2005. However, the primary reference Bauman never discloses said FIFO register priority scheme, at all. Instead, Bauman discloses a "register priority scheme," which was correctly mentioned by the Appellant in said prior Appeal Brief.

Actually, the Appellant asserts that Bauman places packets in its request buffer registers and removes packets therefrom based on either a FIFO priority or a register priority scheme, and every packet in register L0 is serviced first under the FIFO priority scheme. The Appellant further asserts that packets are grouped by type and then placed into specific request buffer registers that are assigned the corresponding packet type in the register priority scheme, and thus, Bauman groups its transfers *prior to placement* within its request buffer registers so that its groups can be inserted into corresponding request buffer registers and can be output from the corresponding request buffer registers in a first in first out basis under the register priority scheme. Therefore, the Appellant argues that Bauman does not teach all the claimed limitations "... associating each entry *after placement* in the queue to one of *a plurality of groups*, each of *the plurality of groups* having a different transaction parameter criteria; determining which particular one of *the plurality of groups* to service based on the transaction parameter criteria; servicing a particular entry in the particular one of *the plurality of groups* based on servicing criteria; ... ."

However, the Examiner believes that the Appellant misinterprets the claim rejection.

First of all, in contrary to the Appellant's assertion, i.e., Bauman places packets in its request buffer registers and removes packets therefrom based on either a FIFO priority or a register priority scheme, Bauman places packets in requests queues 252, 254, 256, 258 (See Bauman, col. 16, lines 44-52) before being grouped into primary arbitration queues 282, 284, 286, 288, which are copies of channel module's request buffers 122, 124, 126, 128 in Fig. 17 (See Bauman, col. 8, lines 32-44). Therefore, Bauman teaches the claim limitation "associating each entry *after placement* in said queue (i.e., requests are placed (viz., enqueued) into requests queues 252, 254, 256, 258, and primary arbitration queues 282, 284, 286, 288 before being grouped into channel module's request buffers 122, 124, 126, 128 in Fig. 17) to one of a

plurality of groups (i.e., each entry being associated with one of channel modules, which has a group of requests for primary arbitration; See Bauman, col. 8, lines 15-32)."

Secondly, all of the other claimed limitations are fully suggested by the combination of Bauman and Trull, which is shown in the above item (9) Grounds of Rejection.

Lastly, in contrary to the Appellant's description on page 8, line 27 through page 9, line 2, i.e., Bauman groups its transfers prior to placement within its request buffer registers so that its groups can be inserted into corresponding request buffer registers and can be output from the corresponding request buffer registers in a first in first out basis *under the register priority scheme,* Bauman teaches that the request groups can be inserted into corresponding request buffer registers and can be output from the corresponding request buffer registers in a priority level (e.g., control, high, medium and low), **not** in a first in first out basis *under the register priority scheme* at col. 8, lines 33-40.

Thus, Appellant's argument for this point cannot be seen as persuasive.

At seventh, the Appellant further asserts that Bauman clearly discloses that requests enter request queues in a time ordered manner with the oldest request being at the bottom of the request queue and the youngest request being at the top of request queue, and any grouping of requests in Bauman is determined prior to placement into a request queue so that the right request can be provided to the right request queue, on page 10, lines 13-32.

However, in contrary to the Appellant's assertion as is stated above, Bauman discloses that requests enter the exemplary request queue 252 in a time ordered manner with the oldest request being at the bottom of the request queue and the youngest request being at the top of request queue, and any grouping of the requests in the request queue into the group of a factor other than time is determined by the queue manager 262 *after placement into the request queue* 252 in Fig. 17. In fact, Bauman is silence as to the Appellant's statement, i.e., any

grouping of requests in Bauman is determined prior to placement into a request queue so that the right request can be provided to the right request queue.

Therefore, the Examiner believes that Bauman suggests grouping of requests being performed after placement into a queue let alone a determination as to which group to service and which entry to service in the identified group being serviced, which is shown in the above item (9) Grounds of Rejection, and Appellant's argument for this point cannot be seen as persuasive.

At eighth, the Appellant states that Trull performs no grouping whatsoever of instructions within its instruction queue, and thus the Examiner has failed to establish the criteria for a prima facie case of obviousness, on page 11, lines 1-17.

Actually, the Appellant argues that Trull does not teach the claimed subject matter "grouping entries after placement into a queue." However, Bauman clearly teaches the argued subject matter "grouping entries after placement into a queue," and furthermore, the combination of Bauman and Trull with rationale suggests the obviousness of the claimed invention.

Thus, Appellant's argument for this point cannot be seen as persuasive.

In response to the Appellant's arguments with respect to "Claim 4 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Bauman, et al. in view of Trull and further in view of Garcia, et al. Independent Claim 1, from which Claim 4 depends, has been shown above to be patentably distinct from the proposed Bauman, et al. - Trull combination. Moreover, the Garcia patent does not include any additional ... Therefore, Applicant respectfully submits that Claim 4 is patentably distinct from the proposed Bauman, et al. - Trull - Garcia, et al. combination." in the substitute Appeal Brief, page 12, the Examiner respectfully disagrees.

In contrary to the Appellant's statement, the independent claim 1 is fully suggested by the combination of Bauman and Trull, and the claim 4 is also suggested by the combination of

Bauman, Trull and Garcia with rationale for proper combination, which is shown in the above item (9) Grounds of Rejection.

Thus, Appellant's argument for this point cannot be seen as persuasive.

In response to the Appellant's arguments with respect to "Claim 8 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Bauman, et al. in view of Trull and further in view of In re Yount. Independent Claim 1, from which Claim 8 depends, has been shown above to be patentably distinct from the proposed Bauman, et al. - Trull combination. Therefore, Applicant respectfully submits that Claim 8 is patentably distinct from the proposed Bauman, et al. - Trull - In re Yount combination." in the substitute Appeal Brief, page 13, the Examiner respectfully disagrees.

In contrary to the Appellant's statement, the independent claim 1 is fully suggested by the combination of Bauman and Trull, and the claim 8 is also suggested by the combination of Bauman, Trull and Case law In re Yount with rationale for proper combination, which is shown in the above item (9) Grounds of Rejection.

Thus, Appellant's argument for this point cannot be seen as persuasive.

In response to the Appellant's arguments with respect to "Claims 9-14 stand rejected under 35 U.S.C. §103(a) as being obvious over Meyers, et al. in view of Bauman, et al. and further in view of Trull. The Examiner has not established that three criteria for a prima facie case of obviousness has been met in this instance." in the substitute Appeal Brief, pages 14-15, the Examiner respectfully disagrees.

At first, the Appellant argues that the Examiner has not shown that Bauman and Trull can be properly combined as proposed let alone for Meyers to be combined with either Bauman

or Trull according to any objective basis in satisfaction of the first criteria, on page 14, lines 12-16.

In contrary to the Appellant's arguments as is stated above, all the rejections under 35 USC §103(a) in the prior Office Actions established a *prima facie* case of obviousness meeting the three basic criteria of the MPEP 2143.03 (8th ed. 2001). Furthermore, the Examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

In this case, the Examiner has clearly pointed out rationale for appropriate combination of Meyers, Bauman and Trull, such that the combination of Meyers and Bauman is for the advantage of memory arbitration scheme (i.e., arbitration method) being that memory arbitration processor (i.e., primary scheduler) is presented with a more diverse arbitration queue (i.e., primary arbitration queue) from which to select transactions (i.e., packets) for transfer through said memory interface (i.e., switch; See Bauman, col. lines 5-8), and further, the combination of Meyers as modified by Bauman and Trull is for the advantage of providing said arbitration queue configured to service transactions (i.e., dispatch instructions) in an out-of-order fashion (i.e., an entry can be removed from any location in the queue) and perform collapse of queue entries (i.e., compaction of strings) of idle locations (i.e., empty storage locations; See Trull, col. 3, lines 48-62 and col. 4, lines 20-23).

Thus, Appellant's argument for this point cannot be seen as persuasive.

At second, the Appellant argues that there has been no mention that the proposed Bauman and Trull combination provides any expectation of success let alone a reasonable

expectation of success, especially with the addition of Meyers to the proposed combination, to satisfy the second criteria, on page 14, lines 16-21.

However, in contrary to the Appellant's assertion, the Examiner finds that because the prior art Bauman teaches that the Appellant's preferred grouping of queue entries is efficient to maximize the throughput of switching queue entries (i.e., cells) without unfairly delaying lower priority data at col. 10, lines 1-6, and provides better results compared with other prior art's processing of queue entries (See Bauman, columns 1-2), and the Examiner further finds that because the prior art Trull teaches that the Appellant's preferred collapsible arbitration queue is efficient to reduce or eliminate the bubbles of empty storage locations form in the queue at col. 4, lines 34-38, and provides better results compared with other prior art's queue compaction, e.g., full compaction (See Trull, col. 18, lines 20-36), there would have been a reasonable expectation of success. In addition, the Appellant fails to present evidence showing there was no reasonable expectation of success. See MPEP 2143.02.

Thus, Appellant's argument for this point cannot be seen as persuasive.

At third, the Appellant asserts that the Examiner readily admits that Meyers fails to teach a collapsible arbitration queue as provided in the claimed invention, and cites Trull to offset this lack of disclosure in Meyers and support a collapsible queue. The Appellant further asserts that Trull places instructions into a queue without associating them with a group, and thus the Examiner cites Bauman for its grouping technique to remedy this deficiency. However, the Appellant argues Bauman groups its transfers prior to placement within its request buffer under the register priority scheme so that each group can be inserted into a specific register and can be output from the specific register in a first in first out basis, on page 14, line 21 through page 15, line 14.

First of all, Bauman places packets in requests queues 252, 254, 256, 258 (See Bauman, col. 16, lines 44-52) before being grouped into primary arbitration queues 282, 284, 286, 288, which are copies of channel module's request buffers 122, 124, 126, 128 in Fig. 17 (See Bauman, col. 8, lines 32-44). Therefore, Bauman teaches the claim limitation "associating each entry *after placement* in said queue (i.e., requests are placed (viz., enqueued) into requests queues 252, 254, 256, 258, and primary arbitration queues 282, 284, 286, 288 before being grouped into channel module's request buffers 122, 124, 126, 128 in Fig. 17) to one of a plurality of groups (i.e., each entry being associated with one of channel modules, which has a group of requests for primary arbitration; See Bauman, col. 8, lines 15-32)."

Secondly, in contrary to the Appellant's description, i.e., Bauman groups its transfers prior to placement within its request buffer *under the register priority scheme* so that each group can be inserted into a specific register and can be output from the specific register in a first in first out basis, Bauman teaches that the each request group can be inserted into a specific request buffer and can be output from the specific request buffer in a priority level (e.g., control, high, medium and low), **not** in a first in first out basis *under the register priority scheme* at col. 8, lines 33-40.

Therefore, the claims 9-14 are fully suggested by the combination of Meyers, Bauman, and Trull with rationale for proper combination, which is shown in the above item (9) Grounds of Rejection, and thus Appellant's argument for this point cannot be seen as persuasive.

In response to the Appellant's arguments with respect to "Claim 15 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Meyers, et al. in view of Bauman, et al. and Trull and further in view of In re Yount. Independent Claim 9, from which Claim 15 depends, has been shown above to be patentably distinct from the proposed Meyers, et al. - Bauman, et

al. - Trull combination. Therefore, Applicant respectfully submits that Claim 15 is patentably distinct from the proposed Meyers, et al. - Bauman, et al. - Trull - In re Yount combination." in the substitute Appeal Brief, page 16, the Examiner respectfully disagrees.

In contrary to the Appellant's statement, the independent claim 9 is fully suggested by the combination of Meyers, Bauman and Trull, and the claim 15 is also suggested by the combination of Meyers, Bauman, Trull and Case law In re Yount with rationale for proper combination, which is shown in the above item (9) Grounds of Rejection.

Thus, Appellant's argument for this point cannot be seen as persuasive.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

CEL/ CEL

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